

***Remarks***

Reconsideration of this Application is respectfully requested. Claims 1-46 are pending in the application, with claims 1, 9, 17, 23, 31, 35 and 38 being the independent claims. Based on the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

***Examiner Interview***

Applicants thank the Examiner for the interview conducted on August 21, 2007. During the interview, Applicants' representatives and the Examiner discussed the present invention, the Office Action and the applied references.

***Rejections under 35 U.S.C. § 101***

Claims 23-30, 45, and 46 were rejected under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter. Applicants respectfully traverse this rejection.

Claims 23-30, 45, and 46 to are directed to a tangible computer readable storage medium such as a computer disk. In 1995, the Commissioner of Patents and Trademarks conceded to the U.S. Court of Appeals for the Federal Circuit “that computer programs embodied in a tangible medium, such as floppy diskettes, are patentable subject matter under 35 U.S.C. § 101.” See *In re Beauregard*, 53 F.3d 1583 (Fed. Cir. 1995). Accordingly, claims 23-30, 45, and 46 to are directed to patentable subject matter under 35 U.S.C. § 101.

On page 17 of the Office Action, the Examiner states that Applicants' prior argument is unpersuasive because "The claim language in light of the specification still encompasses computer usable transmission medium." Applicants respectfully disagree. The claims recite a "*tangible* computer readable *storage medium*." A tangible computer readable storage medium is **not** a transmission medium such as a carrier wave. Accordingly, Applicants have not amended the specification as suggested by the Examiner.

Reconsideration and withdrawal of this rejection are respectfully requested.

***Rejections under 35 U.S.C. § 103***

Claims 1-46 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,167,505 to Kubota (hereinafter "Kubota") in view of Computer Organization and Design by Patterson and Hennessy (hereinafter "Hennessy"). For the reasons set forth below, Applicants respectfully traverse this rejection.

Independent claim 1 recites:

1. An instruction fetch unit for a processor, comprising:
  - a first recoder; and
  - a second recoder coupled to the first recoder,wherein the first recoder passes information regarding a first instruction to the second recoder, and the second recoder recodes a second instruction so as to map the second instruction from a first encoded state to a second encoded state based on the information passed by the first recoder.

Independent claims 9, 17, 23 and 38 recite similar features.

On page 3 of the Office Action, the Examiner alleges that the decoder described by Kubota is equivalent to a recoder. A decoder is **not** a recoder. A decoder decodes an instruction that is in an encoded state and outputs control signals. As described by Kubota:

The instruction decoder circuit 160 decodes each instruction stored in the instruction register 150, and output (*sic*) control signals necessary for the execution of that instruction (*see* Kubota at col. 9, lines 21-23).

As described in specification of the present application, a recoder maps or recodes instructions from one encoded state to another encoded state.

Independent claim 1 recites "the second **recoder** recodes a second instruction so as to map the second instruction from ***a first encoded state to a second encoded state***" (*emphasis added*). Clearly the claimed recoder is not equivalent to the decoder circuit described by Kubota.

The Examiner is improperly construing the term *decoder* to be equivalent to a *recoder*. As described and claimed in the present application, a *recoder* is clearly distinct from a *decoder*. For example, the present application recites:

Instruction recoding unit 208 recodes desired instructions received from instruction staging unit 206. The recoding operation of unit 208 maps instructions from one encoded state (e.g., a 16-bit instruction) to another encoded state (e.g., a 32-bit instruction). ***This is different from the decoding operation performed in pipestage operations 104 (Instruction Decode and Register Fetch) where an encoded instruction is decoded into one or more individual control signals for directing select operations within computer system 100.***  
(*See* Specification at page 7, lines 3-9, *emphasis added*).

As discussed by the Federal Circuit in Phillips v. AWH Corp.:

The claims, of course, do not stand alone. Rather, they are part of "a fully integrated written instrument," Markman, 52 F.3d at 978, consisting principally of a specification that concludes with the claims. ***For that reason, claims "must be read in view of the specification, of which they are a part."*** Id. at 979. As we stated in Vitronics, ***the specification "is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term."*** 90 F.3d at 1582. See *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*emphasis added*)

Furthermore, as stated in M.P.E.P. § 2111.01:

***Where an explicit definition is provided by the applicant for a term, that definition will control interpretation of the term as it is used in the claim.*** *Toro Co. v. White Consolidated Industries Inc.*, 199 F.3d 1295, 1301, 53 USPQ2d 1065, 1069 (Fed. Cir. 1999) (***meaning of words used in a claim is not construed in a "lexicographic vacuum, but in the context of the specification and drawings"***). (See MPEP 2111.01, *emphasis added*)

Because the specification clearly differentiates recoders from decoders, the rejection is improper.

For at least the above reasons, claims 1, 9, 17, 23 and 38 are patentable over Kubota. Hennessy does not overcome the deficiencies of Kubota. Therefore claims 1, 9, 17, 23 and 38 are patentable over Kubota and Hennessy, alone or in combination.

Independent claim 31 recites:

31. A method for recoding instructions for execution by a processor, comprising:

- (a) fetching an expand instruction and an expandable instruction;
- (b) dispatching the expand instruction and the expandable instruction;
- (c) generating at least one information bit based on the expand instruction; and
- (d) recoding the expandable instruction using the at least one information bit generated so as to

map the expandable instruction from a first encoded state to a second encoded state.

Independent claim 35 recites similar features.

For reasons similar to those noted above, neither Kubota nor Hennessy teach or suggest the combination of features recited in claims 31 and 35. Therefore claims 31 and 35 are patentable over Kubota and Hennessy alone or in combination.

Claims 2-8, 10-16, 18-22, 24-30, 32-34, 36, 37, 39-46 depend from one of independent claims 1, 9, 17, 23, 31, 35 and 38 and are patentable for the same reasons as the independent claim from which they depend and further in view of their respective features. For example, claim 3 recites (*emphasis added*):

3. The instruction fetch unit of claim 1, wherein the processor executes instructions having X-bits and belonging to a first instruction set and instructions having Y-bits and belonging to a second instruction set, Y being greater than X, and wherein the first recoder and the second recoder recode an instruction belonging to one of the first instruction set and the second instruction set to form a recoded instruction having at least Y-bits.

In contrast, Kubota teaches fixed length instructions (*see* Kubota at column 2, lines 57-64):

The data processing circuit in accordance with a second aspect of this invention has an architecture such that fixed-length instruction codes are input and executed thereby.

The use of fixed-length instruction codes in this aspect of the invention makes it possible to shorten the time required for decoding the instructions, in comparison with processing involving instruction codes of a variable bit length, and also reduce the size of the data processing circuitry.

Reply to Office Action of May 15, 2007

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Appl. No. 10/698,061

For at least the above reasons, claims 1-46 are patentable over Kubota and Hennessy. Accordingly, the Examiner's rejection of under 35 U.S.C. § 103(a) is traversed and Applicants respectfully request that this rejection be withdrawn.

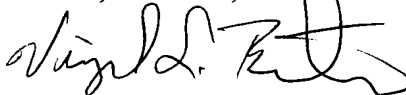
***Conclusion***

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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